AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph on page 10, lines 19-25, as follows:

Referring to Fig. 5, DRAM 10 with logic includes: an interface portion 12 receiving control signals /RAS, /CAS, ..., /CS, an address signal ADD, and data signal DATA; a DRAM 4 operating in accordance with an output from interface portion 12; registers 14, 16 holding data for control in accordance with an output from interface portion 12; and logic circuits 18 and 20 operating in accordance with the data for control respectively held in registers 14 and 16.

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